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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/670,047 | 09/25/2000 | Richard L. Goodson | H-0147 | 4079 |

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| EXAMINER | |
|---|---|
| MERID, ARADOM B | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2631 | 14 |

DATE MAILED: 12/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/670,047 | GOODSON ET AL. | |
| | Examiner | Art Unit | |
| | Aradom B. Merid | 2631 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☐ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 25 September 2000 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1, 2, 4-6, 8-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Choi, U.S. Patent Number: 6,201,832 of Record.

Choi teaches a data detection receiver apparatus that comprises an interpolation filter **20**, an adaptive equalization channel **200,** an analog to digital converter (A/D) **16**, a phase error detector **70**, voltage controlled oscillator (VCO) **180** and a loop filter **80** (Col.5, lines 11-25). The interpolation filter **20** as shown in the fig. 2 is functionally positioned ahead the adaptive equalization channel **200**, and performs interpolation filtering on incoming digital signals to control the timing of the received signals or data (col.6, lines 12-16 and Fig.2) based on the phase error signals successively generated by the phase error detector **70**(col. 5, lines 57-60) as claimed in claim limitations 1.

The adaptive equalization channel **200**, whose coefficients get regularly updated by coefficient updating circuitries **35** and **45**, performs adaptive equalization on the interpolated signals to supply equalized sample value output to the maximum

likelihood sequence detection (MLSD) **60** (col. 7, lines 15-20). The output of the MLSD, as shown in the Fig. 2, is then fed to the phase error detector to update the interpolation filter that uses a look up table processor for selecting a corresponding set of filter of coefficients (col.18, lines 6-9). Therefore, the interpolation filter is correspondingly updated based on the adaptive equalizer output, as in claim limitations 2.

Choi according to Fig. 2 also shows that the phase error detector **70** input signals are functionally linked to the output of the interpolation filter, which controls the timing of incoming signals, pass through the adaptive equalization channel **200**. The phase error detector **70** generates an error signal based on the current data $D_i$ and delayed data $D_{i-2}$ (col. 14, lines 46-50, and claim 8, lines 33-36). The phase error detector **70** which is functionally coupled to the loop filter then outputs the phase error signal to the loop filter **80**. The loop filter performs loop filtering on the phase error signal and thereby provides phase error to the interpolation filter and voltage controlled oscillator (VCO) **180** which is functionally located between the interpolated filter and the loop filter (col. 14, lines 53-59 and Fig, 2) as claimed in claim limitation 4.

And according to Fig. 2, and discussion in the above also the sampled signal pass through the interpolation filter **20** before inputting the received data signal to the phase error detector **70**. Choi as discussed in the above also teaches the method of setting filter coefficients of the interpolation filter using a look up table after receiving phase error signal from the phase error detector signal. Hence the

interpolation coefficients are updated from the look up table based on the filtered phase error output that is generated by the output of the adaptive equalization channel to the phase error detector **70** as claimed in claim limitations 5 and 6.

The incoming analog signal is digitally sampled by the receiver's analog to digital converter (A/D) **16** converter after receiving clock sampling signal from the VCO **180** (col. 15, lines 34 –37) and get interpolated by the interpolation filter **20** to control the timing of the received signal(col.6, lines 12-16). The interpolated samples are then fed to the adaptive equalization channel whose coefficients get updated or adjusted by the coefficient updating circuits **35** and **45** .

The interpolation filter coefficients, as discussed above, are updated based on the phase error output signal that is generated by the phase error detector after receiving equalized output signal from the adaptive equalization channel. Hence the interpolation filter coefficients are correspondingly updated bade on the equalized output. Phase detection is performed on a current and delayed signal to produce a phase error (col. 14, lines 46-50) and passing the phase error through a loop filter to provide signaling to the VCO and interpolation filter. Therefore the above discussion reads on the claim limitation of claim 8-11.

The distorted incoming analog signal is received by the data detection receiver or demodulator and digitized at the sampling clock provided by the VCO **180** to the A/D converter **16** (col. 15, lines 31-36) to produce a stream of digital data . The sampled stream data subsequently gets interpolated by the interpolation filter 20

and equalized by the adaptive equalization channel **200** producing equalized data as claimed in claim limitation 12

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi, U.S. Patent Number: 6,201,832 of Record in view of Cheng et al. U.S. Patent Number: 5,818,378 of record.

Choi as mentioned above discusses how interpolation and equalization are performed by a data detection receiver apparatus that comprises interpolation filter **20**, equalization channel **200,** phase detector **70**, loop filter **80** and VCO **180**. However, Choi fails to provide a means and a method to compensate the time delays and phase distortion due to cable length. Cheng discusses about cable length estimation circuit **110** that provides cable length estimate to the equalizer to compensate the distortion caused by the cable length (see col. 3, lines 34-38). Thus adding a cable length estimation circuit of Cheng's invention to the data detection apparatus of Choi' s invention to provide the interpolation filter **20** with

cable length coefficients to compensate the distortions due to cable length would have been obvious to a person with an ordinary skill in the art during the time of the invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aradom B. Merid whose telephone number is 703-305-8953. The examiner can normally be reached on 8:00am-5:00pm (Mon. - Fri.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohamed Ghayour can be reached on 703-306-3034. The fax phone number for the organization where this application or proceeding is assigned is 703-308-9051.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Aradom B. Merid

M. Gf
MOHAMMAD H. GHAYOUR
PRIMARY EXAMINER